

W2S Semínar (Webínar seríes on Spíntronics)



Scalable Probabilistic Computing with Magnetic Tunnel Junctions

Speaker:

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Abstract

Digital computing is based on the notion of a "bit" which is a deterministic "0" or "1". Quantum computing is based on the notion of a "qubit" which can be a superposition of "0" and "1". In this talk, I will draw attention to something in between, which we call a probabilistic or p-bit that can be used as a building block to build probabilistic computers. A particularly compact implementation of p-bits comes from spintronics: The natural noise in a magnetic tunnel junction (MTJ) in combination with a CMOS transistor leads to a highly compact and energy-efficient p-bit. I will discuss our recent table-top experiment implementing 8 such interconnected MTJ/CMOS p-bits that run asynchronously to solve a class of optimization problems. I will also show scaled CMOS-based emulators of such asynchronous p-computers using thousands of p-bits to illustrate the device and architecture level promise of extreme-scale implementations with spintronics.

To attend the lecture please visit Zoom link: <u>https://us06web.zoom.us/j/93788522063</u> <u>Contact:</u> Dr. Subhankar Bedanta (Convenor W2S) Email: w2s-spintronics@niser.ac.in

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