STUDY OF LOCK-IN AMPLIFIER

I: LOCK IN AMPLIFER

1. INTRODUCTION:

The lock-in amplifier is a device, which can measure very small AC voltages in the presence of noise. It uses the principle of phase sensitive detection. It produces a maximum DC output when the signal to be measured is in phase with a reference signal at the same frequency. This in-house built lock-in amplifier using AD630 chip is low cost and for the teaching purpose of phase sensitive detection. It has limited frequency and input voltage ranges of about frequency range 200 Hz to 2 kHz and input voltages of few microvolts.

2. DESCRIPTION OF THE FRONT PANEL

The mains switch is at corner of the back panel. When the switch is pressed down the lock-in amplifier is powered and an indicator light in the switch comes on. On the front panel left side there are input banana sockets for signal and reference and on the right half of the front panel there are BNC sockets for DC output (V_O DC), amplified signal, PIN13 of AD630 output, amplified Reference (REF) and amplified phase shifted Reference (REF'), reference signal is phase shifted by turning the knob of a POT(potentiometer) marked PHASE ADJ. The BNC socket marked SIGNAL can be connected to an oscilloscope to show the amplified small AC signal with noise. BNC socket 'PIN13' is to observe the output at PIN13 of AD630 IC which is used for phase sensitive detection in this lock in amplifier. As the phase shift adjust (PHASE ADJ.) knob is turned the pattern of the output at PIN13, as seen on an oscilloscope, changes. The BNC pin marked 'V_O DC' (DC output) is connected to a DMM in an appropriate DC range. This measures the amplified DC output from PIN13 of the AD630 chip.

Figure I. Lock-in Amplifier front panel

There is knob with potentiometer DC OFFSET ADJ, it is for continuous adjustment the DC offset in the otherwise AC input signals. There is another selector knob SIGNAL GAIN and it is for setting gain of the SIGNAL. GAIN has options of 5,10, 100, 500 and 3000. Gain of 50 and 100 are used in this experiment. **Extreme left position of the knob denotes Gain 5**.

PRINCIPLE OF PHASE SENSITIVE DETECTION

A. INTRODUCTION

Normally amplifiers have a bandwidth of several kilohertz. There are different sources of noise in an amplifier. The flicker noise is present in all electronic instruments and its power spectrum varies inversely with the frequency. This noise becomes a problem only if one works at very low frequencies. Then we have noise due to electromagnetic pick up from running motors, tube lights and so on. Such a noise has a peak in the power spectrum only at the frequency of the motor or the frequency of the mains. Such noise can be reduced by electromagnetic shielding. The third source of noise is thermal noise. This is of thermodynamic origin and cannot be avoided. Its power spectrum extends over all frequencies. So it is called white noise. If we have resistance 'R' through which a current, 'I' is flowing the voltage across the resistance will vary randomly about the average value $V_0 = IR$. The mean square fluctuation of the voltage is defined by $< (V-V_0)^2 >$ where the average is taken over a

long period of time. If we measure the noise over a bandwidth W, the mean square voltage will be

$$< (V-V_0)^2 > = 4\, k_B\, T\, R\, W \qquad \text{(II.9.1.1)}$$

To reduce this noise, we either reduce the temperature T or reduce the bandwidth W of the amplifier. For detecting very weak signals at room temperature we have to effectively reduce the bandwidth to a few Hertz though the amplifier has a large bandwidth in kilohertz range. This is achieved by Phase Sensitive Detection.

B. SIGNAL AND REFERENCE

Let us have an AC sinusoidal cause. The cause may be the current through the primary coil of a mutual inductance. It may be a light signal whose intensity is modulated periodically. This cause will have an effect that will have the same frequency as the cause but may differ in phase from the cause. The effect in the case of the mutual inductance is the induced emf in the secondary coil. This will be 90^0 out of phase with the current in the primary coil, but it will have the same frequency as the current. The effect will be weak of the order of a few micro volts or nanovolts. If we merely amplify the weak signal a million times we will also amplify the noise. In an ordinary amplifier the noise is collected over a wide frequency range and so may even swamp the weak signal due to the cause.

To overcome the noise vis-à-vis the weak effect signal, we take a reference signal, which is derived from the cause signal and is in phase with it. For example, in the mutual inductance, a resistance is connected in series with the primary coil so that the current through the primary also passes through the resistance R. The voltage across the resistance will be the reference signal. By choosing R suitably one may generate a reference signal of a few tens of a millivolt or more.

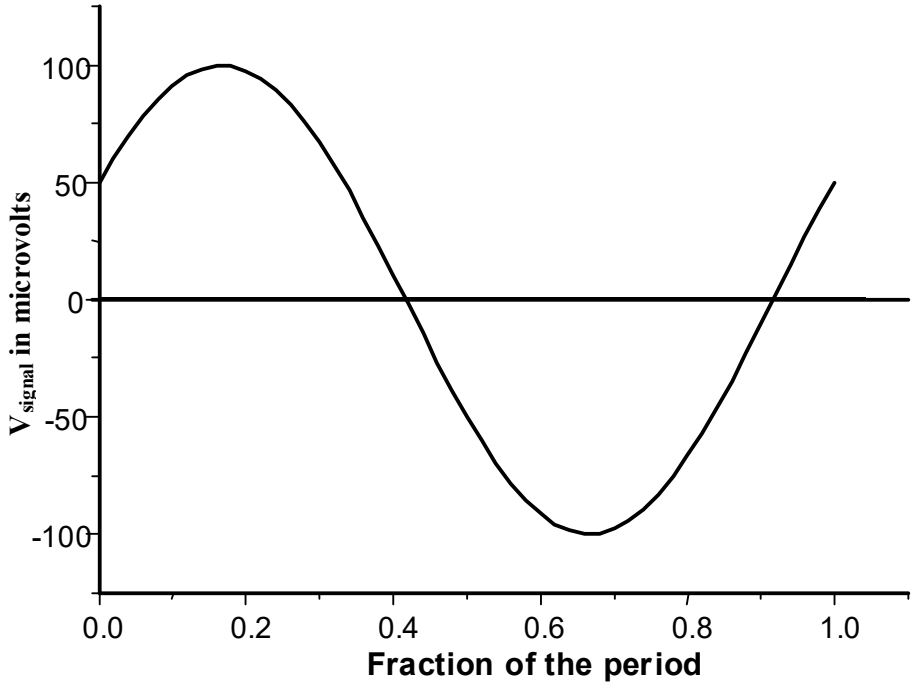


Figure II. Weak signal as a function of time (t/T) where T is the Period.

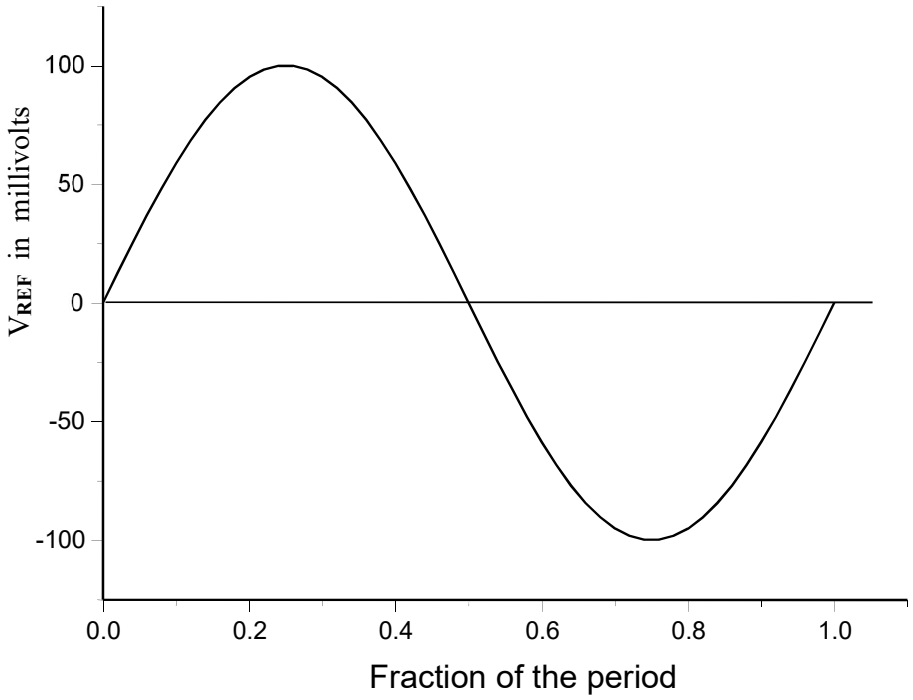


Figure III Reference voltage as a function of time (t/T) where T is the Period.

From the above figure it is seen that the weak signal is advanced in phase relative to reference signal by an angle ϕ. In the above example $\phi = \pi/6$.

We may write

$$V_{signal} = V_0 \sin(\omega t+\phi) \qquad \text{(II.9.1.1)}$$

and

$$V_{ref} = V_0 \sin(\omega t) \qquad \text{(II.9.1.2)}$$

Let us say these are the magnitudes of the signal and reference voltage after some amplification in our circuit.

These signals are then fed to the chip AD 630. This is a phase sensitive detector. In this chip there are two identical amplifiers. One is a noninverting amplifier. This means that the output is in phase with the input. The other is an inverting amplifier i.e. the output is 180^0 out of phase with the input. There is a switch operated by a comparator. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion The comparator senses the reference signal. When the reference signal is positive (i.e. for time t $0<t<T/2$) the comparator connects the weak signal V_{signal} to the direct amplifier so that the output of the amplifier is

$$V_{out} = \mu V_{signal} \qquad 0<t<T/2 \qquad \text{(II.9.1.3)}$$

When the reference signal is negative (i.e. for time t between T/2 and T) the weak signal is connected to the inverse amplifier so that the output voltage is

$$V_{out} = -\mu V_{signal} \qquad T/2<t<T \qquad \text{(II.9.1.4)}$$

Figure (IV) shows the amplified signal V_{out} assuming an amplification of 1000.

We see from Figure IV that the output signal is positive for most of the period but there is a small negative portion. So the output signal will have an average DC part superposed on an AC part at the frequencies ω, 2ω …. If we have a filter that will bypass the AC components to earth, we will get a DC output V_{DC}. We may calculate the DC output from the equation

$$V_{DC} = (1/T)\left\{\int_0^{T/2} \mu V_0 \sin(\omega t+\phi)dt - \int_{T/2}^{T} \mu V_0 \sin(\omega t+\phi)dt\right\} \qquad \text{(II.9.1.5)}$$

$$= \{4\mu v_0/2\pi) \cos(\phi) \qquad \text{(II.9.1.6)}$$

remembering $\omega T = 2\pi$.

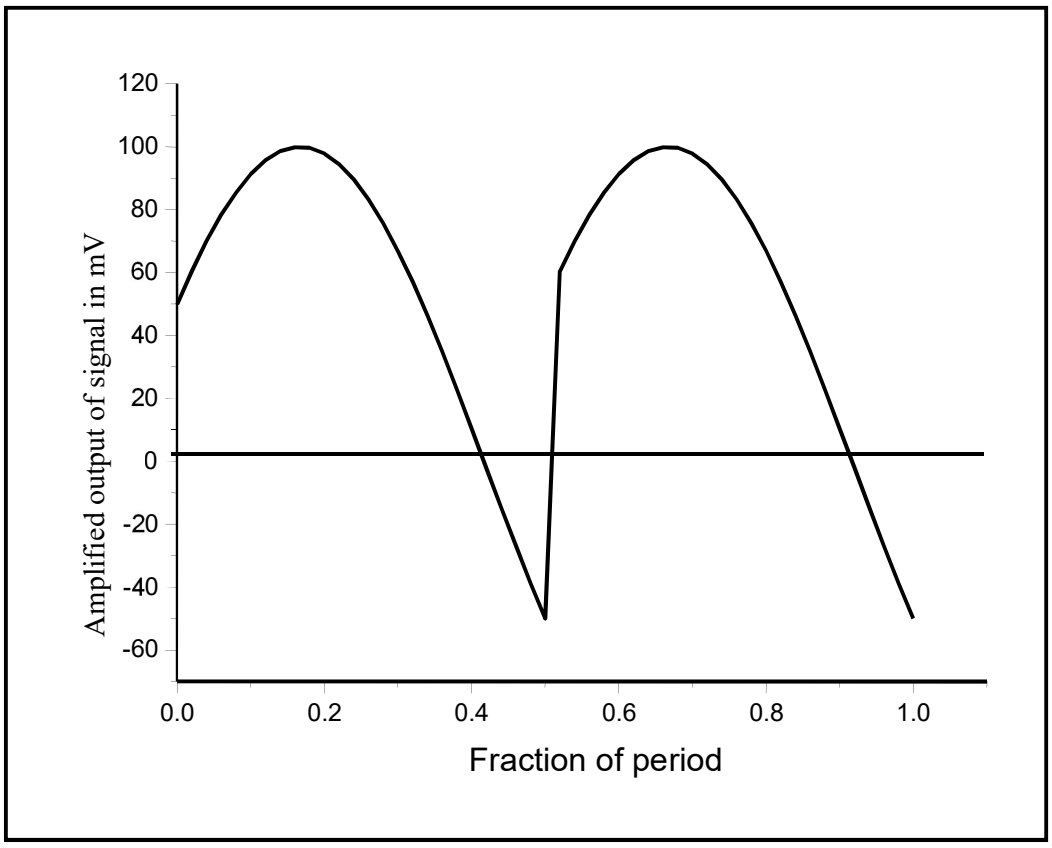


Figure IV Amplified output V_{OUT} when the reference signal is fed to the comparator.

If we introduce a circuit to phase shift the reference signal and then send the phase shifted reference signal to the comparator in AD 630, the output DC voltage will vary as the phase shift is increased from zero. It will reach a maximum when the reference signal is phase shifted by ϕ and the phase-shifted reference signal is in phase with the weak signal $V_{signal.}$ Then the output voltage will look like the one shown in Figure V. The average DC voltage V_{DC} will then reach a maximum value $2\mu V_0/\pi$.

That is why we call this phase sensitive detection and the amplifier a lock in amplifier because we make the weak signal lock in phase with the phase-shifted reference to give maximum DC output voltage. If we measure on an oscilloscope how much we have to shift the phase of the reference signal to get maximum DC output that gives the phase difference between effect and cause.

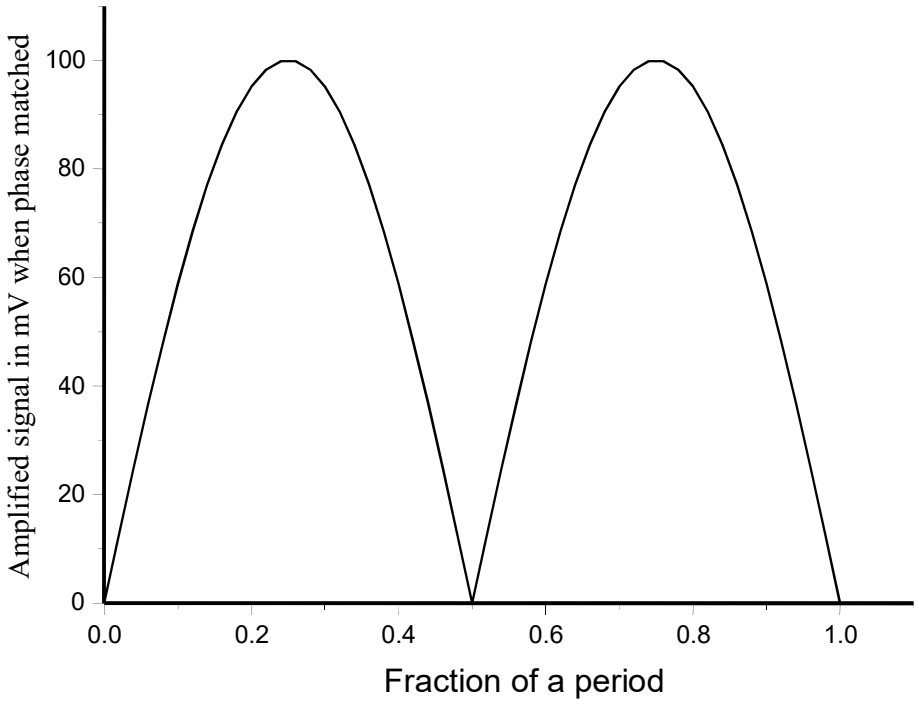


Figure V: Amplified output signal when the reference signal is phase Shifted by ϕ and fed to AD630 chip

Suppose we have noise at a frequency ω' different from the frequency ω of the reference signal. We have a large integration time (several times the period of the reference signal). Then we can show that the contribution of this noise to V_{DC} drops rapidly as ω' differs from ω. If 'τ' is the integration time large compared to the period of the reference signal, then only noise frequencies differing from ω by n/τ (where n is a small number) will make a contribution to V_{DC}. This means that the effective bandwidth of the lock-in amplifier is n/τ. If the integration time is 1 second, this implies that the effective bandwidth W is a few Hz. So one can understand how thermal noise and other noises are suppressed by the lock-in amplifier.

II. CALIBRATION OF THE LOCK-IN AMPLIFIER

1. INTRODUCTION:

In Section I, a lock-in amplifier is described. Before using the lock-in amplifier for experiments, one must calibrate the lock-in amplifier. Calibration means measuring the maximum output DC voltage of the lock-in amplifier for different small AC signal voltages as a function of the frequency of the signal.

2. APPARATUS REQUIRED:

Signal generator, lock in amplifier, two channel oscilloscope and a DMM.

3. PROCEDURE

1) Make a voltage divider circuit on bread board using 4.7 kΩ and 12 Ω to generator reference and signal voltages for calibration. Give input voltage to voltage divider using signal(function) generator. Reference is taken across 4.7 kΩ and signal is taken across 12 Ω and connect them using cables to lock in amplifier.

2) Set the frequency of the signal generator at 300 Hz. Adjust the amplitude V_{APP} (V_{PP}) of the signal generator at about 1 V.

3) The voltage across 12 Ω will be V_{SIG}

$$V_{SIG.RMS} = V_{APP.RMS} \text{ x } 12/ (4712) = 0.0025V_{APP.RMS} \text{ V} \qquad \text{(II.9.2.1)}$$

The reference voltage is the voltage across the 4.7 kΩ resistor

4) Connect the BNC sockets marked REF. and REF‘ to the two channels of an oscilloscope. Set the GAIN as 50 on lock in amplifier. There will be two sinusoidal traces at the frequency of the signal generator. These are amplified reference signals, one before phase shifting and the other after phase shifting. Since the phase shift is zero when the phase adjusting pot is at the extremt, the two traces can be superposed exactly indicating zero phase shift. Note the DC volts on a DMM connected to the V_O DC. This DC voltage will be positive. Turn the phase shifter potentiometer knob anti-clockwise and observe what happens to the signal coming from REF’ relative to the signal coming from REF. You will see that the signal from REF’ moves to the right relative to the signal from REF. This indicates a phase shift between the two signals. Note that as you turn the knob the DC voltage on the multimeter comes down. Turn the knob and adjust to the position when the DC voltage on the multimeter is zero. You will see that the maxima of the REF’ signal now occur at the position of zeroes of the REF Signal. This indicates a phase shift of 90^0. You can check this by feeding the two signals to the X and Y plates

of the oscilloscope and noting that the Lissajous pattern is a circle on the oscilloscope. (There is distortion of the reference signal after phase shifting. So the circle will be distorted.) If the knob is turned further, the phase shift increases beyond 90^0, the panel meter reading becomes negative. When the knob of the phase shift potentiometer is to the left end the phase shift is nearly (but less than) 180^0 and the panel meter indicates the negative largest value.

In the calibration circuit, the signal and reference voltages are derived from the potential differences across two resistances in series. They are in phase. So the panel meter voltage is largest when the phase shift is zero.

Connect the BNC socket marked PIN 13 to the oscilloscope and see how the output of the lock-in chip changes as the phase shifter knob is turned. As the knob is turned the output at PIN 13 develops a larger and larger negative part.

You can also observe the signal output on the oscilloscope and phase difference between signal and REF or REF'. But after observing keep back them to arrangement of Lissajous figures with REF and REF'.

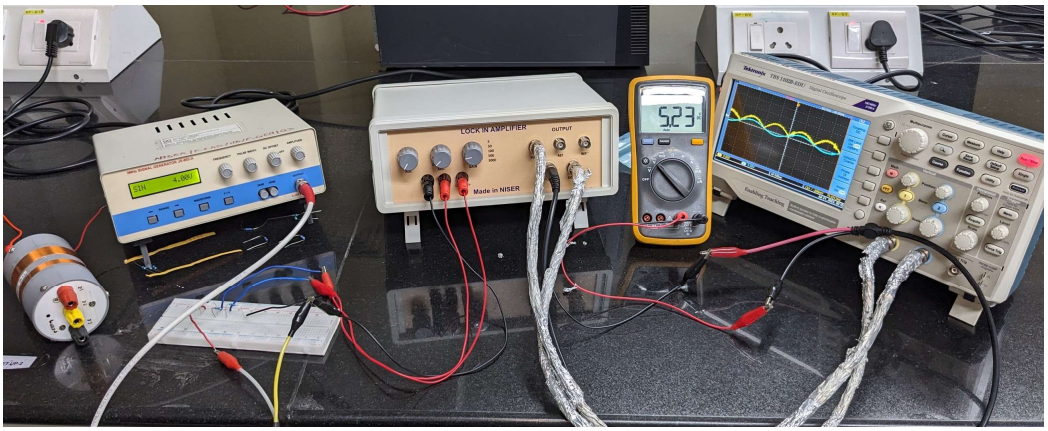
5) Turn the phase adjustment potentiometer knob to the right extreme and wait till the DMM connected to the output socket of the lock in shows a steady DC value. At the extreme end of the knob the phase difference between the signal and the reference is zero. Note the reading on the DMM. This is called V_{DC}.

6) Repeat operations 6 for various values of the output of the signal generator (or applied input to the circuit) from 1 V_{PP} to 3 V_{PP} in steps of 0.5 V_{PP}, keeping the frequency fixed.

7) Plot V_{DC} vs. V_{SIGRMS} calculated from V_{APP} using equation (II.9.2.1). Find the slope μ. This is the amplification factor at this frequency f.

8) Change the frequency from 300 to 1500 Hz insteps of 300 Hz. At each frequency repeat step (7).

9) Repeat the above steps and take readings with GAIN 100.



FigVI. Arrangement of lock in amplifier experiment

Table II.9.2.1
Calibration of the Lock-in-amplifier (use RMS values and calculate for both GAIN of 50 and 100)

f Hz →	300		600			900		
Volts	μV	Volts	Volts	μV	Volts	Volts	μV	Volts
V_{AC}	Vsig	V_{DC}	V_{AC}	Vsig	V_{DC}	V_{AC}	Vsig	V_{DC}
f Hz →	1200		1500					
Volts	μV	Volts	Volts	μV	Volts			

Table II.9.2.2 Amplification factor μ at different frequencies for both the GAIN

f (Hz)	μ	Error in μ

III.MUTUAL INDUCTANCE WITH LOCK- IN-AMPLIFIER

1. INTRODUCTION

When two coils are placed side by side and an AC current is passed through one coil (called the primary), an AC voltage at the same frequency is induced in the other coil (called the secondary). If the primary current varies as

$$I = I_0 \sin(2\pi f t) \qquad \text{(II.9.3.1)}$$

where f is the frequency in Hertz, the emf induced in the secondary is

$$V = -M\, dI/dt = -2\pi M f I_0 \cos(2\pi f t) \qquad \text{(II.9.3.2)}$$
$$= -2\pi M f I_0 \sin(2\pi f t + \pi/2)$$

So

(1) The phase difference between the primary current and the induced emf is $\pi/2$
(2) The emf is proportional to the amplitude I_0 of the current
(3) The emf is proportional to the frequency f.

In this experiment all these factors will be verified using the lock in amplifier.

2. THE MUTUAL INDUCTANCE COIL

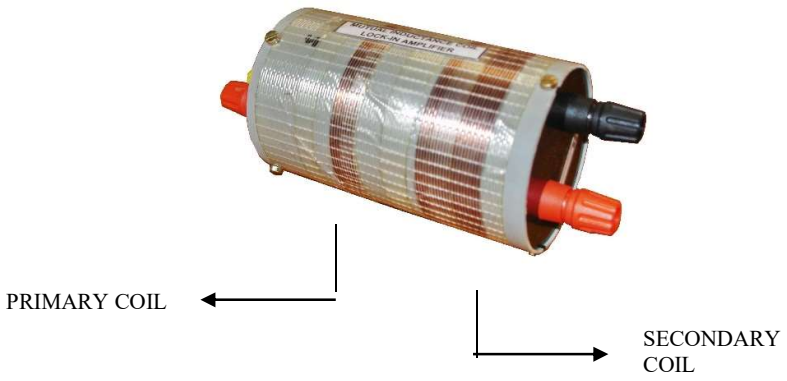


Figure VII. Mutual inductance coils

On an insulating former a coil of about 20 turns is wound using insulated copper wire, which can carry a current of about a few milli-ampere. There are three banana terminals Red, yellow and black at one end of the coil. A 4.7 kΩ resistor and the primary coil are connected between red and yellow banana terminals. Between the yellow and black a 100 Ω resistor is connected. When a signal generator is connected between the red and black terminals and a rms AC voltage of V volts is applied, a rms current of

$$I_{RMS} = V_{RMS}/R_{Total} = V_{RMS}/4.8.x10^3 \text{ amps} \qquad (II.9.3.3)$$

flows through the primary coil. The resistance of the primary coil, which is of the order of 1 Ω, is neglected in the denominator compared to 4800 Ω. The voltage across 100 Ω be used as the reference signal. The signal generator ground must be connected to the black terminal on the primary side of the coil box and the other terminal of the signal generator must be connected to the red banana terminal on the primary side of the coil box.

On the same former a second coil of about 100 turns is wound at a distance of a few centimeters from the end of the primary coil. The terminals of the secondary coil are brought to two banana terminals on the other end of the insulating former. The emf generated by mutual inductance of the coils will appear at these terminals and will be measured by the Lock in amplifier.

3. APPARATUS REQUIRED

Signal generator, lock in amplifier, two-channel oscilloscope, mutual inductance coil and one DMM to measure DC output of lock in amplifier.

4. PROCEDURE

The red terminal on the signal generator is connected to the red terminal and the black terminal on the signal generator to the black terminal on the primary coil side of the insulating former. Connect the two terminals (Yellow and Black) on the primary coil side of the insulating former to the BANANA socket marked **REF** I/P on the front panel of the LIA.

Connect the red terminal on the secondary side of the insulating former to the red banana terminal marked **SIG I/P** on the LIA. Connect the black terminal on the secondary side of the insulating former to the black banana terminal marked **SIG I/P** on the front panel of the LIA.

Connect a DMM the BNC socket marked OUTPUT on the front panel of the LIA. Connect the two BNC sockets marked REF and REF' on the front panel of the LIA to the two channels of an oscilloscope.

IMPORTANT: If all the instruments do not have a common ground the readings on the DMM will fluctuate wildly.

Switch on the signal generator. Set the amplitude (V_{PP}) to about 7 Volt and the frequency to about 600 Hz. Set the GAIN as 100. Switch on the Lock in Amplifier and the oscilloscope. You will see two sinusoidal traces at the frequency of 600 Hz on the oscilloscope. When the phase shift adjust pot on the LIA is to the extreme right the

two traces will be in phase. Note that the DMM reading is small. Now turn the phase adjust pot to the left. The trace of REF' will shift relative to the trace of REF and the DMM reading will increase. The DMM takes some time to reach a steady value. So turn the phase adjusting pot little by little and wait for the DMM to reach a steady reading. The magnitude of the reading on the DMM will increase and reach a maximum at one position of the phase adjusting pot. A further turning of the phase adjusting pot will reduce the magnitude of the reading. Keep the phase adjusting pot at the position when you get the maximum reading on the DMM. On the oscilloscope screen we see that the phase difference between the two traces is 90^0. **To show this more dramatically press the XY button on the oscilloscope. Now one sees the Lissajous figure due to the signals Ref and Ref'**. When the DMM shows the maximum value this figure on the oscilloscope screen is a circle. The reference signal is in phase with the current. A maximum output of the LIA indicates that the phase-shifted reference signal is in phase with the mutual inductance emf. The Lissajous figure shows that the phase-shifted reference is 90^0 out of phase with the reference signal. **SO THE MUTUAL INDUCTANCE EMF IS 90^0 OUT OF PHASE WITH THE PRIMARY CURRENT.**
(NOTE: Circle may be distorted due to distortion of REF'. If there is a large distortion of the phase shifted REF' signal the Lissajous Figure may appear more like a square with rounded corners.)

Note the DMM reading. Keeping the frequency of the signal generator the same, change the amplitude from 7 to 15 V (V_{PP}) in steps of 2 V. Note that there is no need to adjust the phase shift pot for each amplitude at a given frequency. Once the phase shift is adjusted to get a circle as the Lissajous figure on the oscilloscope screen, changing the amplitude only changes the radius of the circle but does not change its shape.

Having taken the readings of the DMM for different signal generator amplitudes at 600 Hz, repeat the experiment at different frequencies in steps of 300 Hz till 1500 Hz. When the frequency is changed the phase-shift pot needs to be adjusted to get the maximum magnitude for the DMM reading.

Table II.9.3.1 Applied voltage to the circuit with signal generator (V_{AC}) and the DC output voltage of the Lock in Amplifier (V_{DC}) in volts (USE RMS values for $V_{AC} = V_{PP}/2\sqrt{2}$)

600 Hz		900 Hz		1200 Hz		1500 Hz	
V	V	V	V	V	V	V	V
V_{AC}	V_{DC}	V_{AC}	V_{DC}	V_{AC}	V_{DC}	V_{AC}	V_{DC}

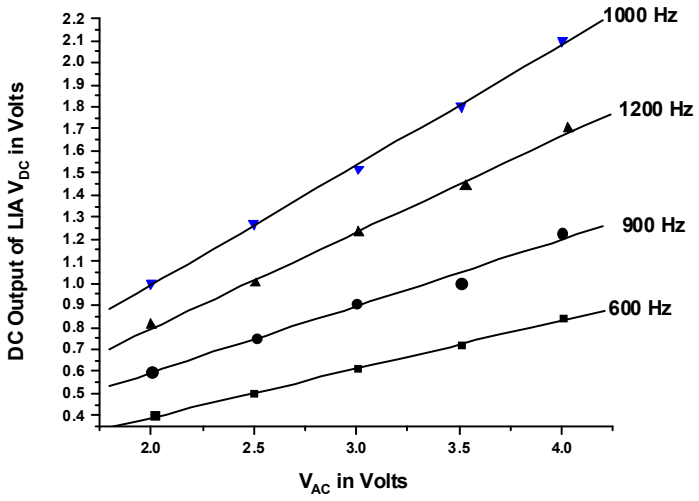


Figure VIII: Example graph of DC output of LIA versus AC(RMS) voltage applied to primary circuit

The slopes of these curves at different frequencies are given in Table II.9.3.2.

Table II.9.3.2

f (Hz)	Slope

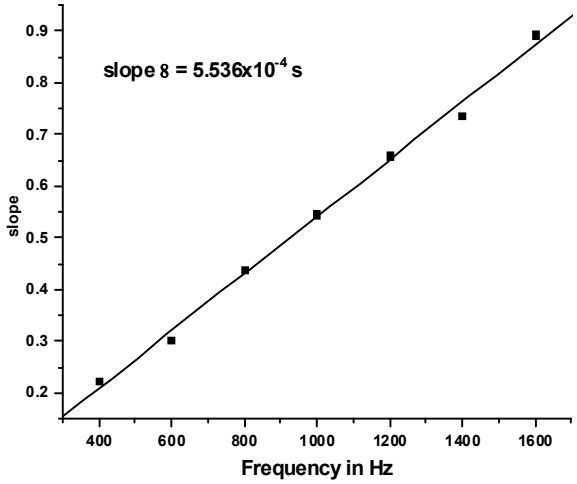


Figure IX. Example plot of 'slope of V_{DC} vs V_{AC} RMS curves' in Figure VIII plotted against frequency

This curve is linear with a slope 5.536×10^{-4} s. The figures VIII and IX show that the mutual inductance emf is proportional to the current through the primary coil and to the frequency of the AC current.

The slope β of the graph in Figure IX must be equal to

$$\beta = 2\pi M\mu/R \qquad \text{(II.9.3.4)}$$

Where M is the mutual inductance of the coil, μ is the amplification factor of the LIA and R is the resistance in the primary circuit (4.8 kΩ). Substituting all the values in (II.9.3.4) Calculate M.

You learn from this experiment that:

1. The mutual inductance EMF is 90^0 out of phase with the current in the primary coil
2. The EMF is proportional to the current in the primary coil
3. The EMF is proportional to the frequency.

[NOTE: The mutual inductance will vary from coil to coil. Since it depends inversely on the third power of the distance between the primary and secondary coils the variation will be appreciable. The above readings are sample readings only.]

IV. MEASUREMENT OF LOW RESISTANCE

1. INTRODUCTION:

Measurement of low resistance (resistance less than an Ohm) with the DC technique would require a high current. Also since the voltage developed across the resistance will be small, it will be affected by broadband noise when it is amplified.

The AC technique using a lock-in-amplifier provides a solution to the problem. This is illustrated by the following experiment.

2. Arrangement for measuring resistance of low resistor. Make a voltage divider circuit on bread board using 500 Ω and given low resistor. Input voltage from signal generator is applied across all the resistances connected in series. Reference is taken across 500 Ω and signal is taken across the low resistor and connect them using cables to lock in amplifier.

3. APPARATUS REQUIRED

Signal generator, lock in amplifier, two-channel oscilloscope, low resistance box and one DMM to measure output of lock in amplifier

4. PROCEDURE:

The output terminals of the signal generator are connected to the two end of voltage divider circuit made on bread board using above components. Connect the voltage across low resistor to the banana terminals marked **SIG I/P** on the Lock-in amplifier front panel. Connect voltage across 500 Ω to **REF I/P**. The black output terminal of the signal generator is also connected to the terminal marked GND on the front panel of the Lock-in amplifier via bread board. This ensures a common ground between the signal generator and the LIA. Connect the socket marked OUTPUT on the front panel of the LIA to a DMM.

Switch on the signal generator. Adjust its frequency to be about 300 Hz and its amplitude to 1 V (V_{PP}). Switch on the lock in. A DC voltage will appear on the DMM which will reach a positive maximum value as the phase adjust pot is turned to almost the right extreme position. Note the value of this maximum DC voltage V_{DC}. Change the signal generator output V_{AC} in steps of 0.5 V up to 3 V and each time adjust the phase adjusting Pot of the LIA slightly to get maximum voltage on the DMM and note this voltage V_{DC}. Repeat the experiments at frequencies, till 1500 Hz in steps of 300 Hz.

At each frequency plot a graph between V_{DC} and V_{AC}. Fit the points to a straight line and get the slope dV_{DC}/dV_{AC}.

$$dV_{AC} = R\, dI_{AC} \qquad \text{(II.9.4.1)}$$

R is the total resistance in the primary circuit (4.8 kΩ) and dI_{AC} is the change in the current through the low resistance when the signal generator voltage is changed by dV_{AC}. The output DC signal V_{DC} is proportional to the voltage V_r across the low resistance r. When the current through the low resistance is changed by $dI_{AC,}$ the voltage V_r changes by dV_r
where

$$dV_r = r\, dI_{AC} \qquad \text{(II.9.4.2)}$$

and this causes a change in V_{DC} by dV_{DC} given by

$$dV_{DC} = \mu dV_r = \mu r\, dI_{AC} = (\mu\, r/R)\, dV_{AC} \qquad \text{(II.9.4.3)}$$

So $$dV_{DC}/\, dV_{AC} = (\mu\, r/R) \qquad \text{(II.9.4.4)}$$

To ensure that the contribution to V_r from residual inductance of the low resistance is small, we work at low frequencies and we check that the slope dV_{DC}/dV_{AC} is independent of the frequency.

Table II.9.4.1
Low resistance measurement (use RMS values for V_{AC})

300 Hz		600 Hz		900 Hz		1200 Hz		1500 Hz	
V_{AC} V	V_{DC} V	V_{AC} V	V_{DC} V	V_{AC} V	V_{DC} V	V_{AC} V	V_{DC} V	V_{AC} V	V_{DC} V

The slopes for all frequencies are collected in Table II.9.4.2.

Table II.9.4.2

Frequency (Hz)	Slope

From the average slope calculate the low resistance (r) from the formula II.9.4.4.

Questions:

1. If I increase the number of turns in the secondary coil will the mutual inductance increase or decrease? Give a reason.
2. Keeping the number of turns constant in the primary coil, I increase the length will the mutual inductance increase, decrease or remain a constant? Give a reason for your answer.
3. If the distance between the primary and secondary coils is increased will the mutual inductance increase or decrease? Give a reason.
4. If the frequency of the signal is decreased what will happen to the induced EMF in the secondary for the same current in the primary?
5. To get a DC signal voltage of 1 volt what should be the current through the primary coil in the Mutual inductance set up at a frequency of 500 Hz?
6. If you directly measure the resistance of jumper wire with multimeter, do you get the resistance? Explain your answer.
7. What is the heat dissipated in the low resistance when V_{AC} is 2 V?
8. If the inductance of the coil is 1 micro-Henry, what will be the contribution of the inductance to the voltage V_r at a frequency of 10 kHz? What will be the sources of error in this case?